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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,517	02/12/2002	Mark Templeton	ARTCP031	6733

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EXAMINER	
BAKER, STEPHEN M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,517	TEMPLETON ET AL.	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *040703*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,230,290 to Heidel *et al* in view of U.S. Patent No. 5,764,878 to Kablanian *et al* (hereafter Kablanian).

Heidel discloses arrangements for performing "high stress" built-in self-testing (BIST) for a DRAM chip. The chip can also any other type of volatile or non-volatile memory, e.g. SRAM, SDRAM, EEPROM, etc. An "internal clock signal for use in accessing a memory array" is generated (col. 2, lines 32-51) by a clock generator unit (102), with either one of a row internal control signal (RINT) and a column internal control signal (CINT) serving as the "internal clock signal" in Heidel's memory. Heidel refers to these signals (RINT, CINT) as "control clocks" (col. 3, line 27) although they are more commonly referred to as "strobes". During BIST operation only, an internal control signal generating unit (4208) of BIST logic (4202) generates the DRAM internal signals (RINT or CINT) instead, to provide a "stress clock signal" for "performing a built-in self-test of the memory array using a stress clock signal, wherein each pulse of the stress clock signal is of shorter duration than each pulse of the internal clock signal".

Heidel's internal control signal generating unit (4208) generates the "stress clock signal" responsive to a BIST system clock generator (4220). During the stress testing, instead of passing DRAM control clocks, the clock generator unit (CLKGEN 102) generates a clock input to the BIST system clock generator (4220) (col. 3, lines 36-38). Internal signal timings for the tests are stored in a Timing Table (4218), and when a test is passed, the timing parameter may be tightened to create a more severe timing condition (col. 6, lines 26-28), enabling the determination of design timing margins.

Heidel's testing is used to grade the chips into various performance ranks. As Heidel does not disclose any built-in self-repair capability for the memory array, Heidel does not show any means specific to "storing defective memory addresses" of defective memory cells detected by Heidel's memory array stress tests, nor any means specific to "redirecting memory access operations to ... redundant memory cells".

Kablanian discloses a memory array with built-in self-repair (BISR) in addition to BIST. In a manner typical of BISR for a memory array, Hablanian provides means for "storing defective memory addresses detected by the built-in self-test in a memory block" and means for "redirecting memory access operations to ... redundant memory cells" during normal operation. BISR provides Kablanian's memory array chip with the well-known benefit of increasing the number of usable chips.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to enhance Heidel's BIST memory chip with the typical BISR memory chip features shown by Kablanian, including a means for "storing defective memory addresses detected by the built-in self-test in a memory block" and a means for

"redirecting memory access operations to ... redundant memory cells". Such enhancement would have been obvious because BISR provides the well-known benefit of increasing the number of usable chips.

Regarding claims 2 and 17, Kablanian discloses a latch "register' for storing defective memory addresses (col. 6, line 48).

Regarding claims 9 and 18, Kablanian shows "redundant control logic that redirects memory access operations to the defective memory addresses to redundant memory cells" (Fig. 9).

Regarding claims 4, 10, 11, 19 and 20, Heidel's normal "internal clock signal" (RINT or CINT) is presumably "based on a margin added to the required read and write times" as applying external signals (XRAS, XCAS, XWE) to a memory chip in such a manner as to include a timing "margin" is understood to be conventional practice.

Regarding claims 5, 12 and 21, Official Notice is given that establishing an "optimal margin" for applying external signals (XRAS, XCAS, XWE) to memory chips, in such a manner as to accommodate worst case environmental conditions and operating conditions, was conventional practice at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to apply Heidel's normal "internal clock signal" (RINT or CINT) with an "optimal margin". Such operation would have been obvious because establishing an "optimal margin" for applying external signals (XRAS, XCAS, XWE) to memory chips, in such a manner as to accommodate worst case environmental conditions and operating conditions, was already conventional practice.

Regarding claims 6, 13 and 22, as timing variations used during Heidel's BIST procedure cover a range of timings including those capable of triggering memory errors, a timing that "is approximately equal to each pulse of the (normal) internal clock signal minus the margin" is apparently generated.

Regarding claims 15 and 23, Official Notice is given that designing a chip by means of a "generator", such as a CAD system, was conventional practice having well-known advantages at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to generate a chip having the combination of features cited above by means of a "generator". Such a process would have been obvious because designing a chip by means of a "generator", such as a CAD system, was already conventional practice having well-known advantages.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (703) 305-9681. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen M. Baker
Primary Examiner
Art Unit 2133

smb